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U1S S2090

(56) Documents Cited
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(58) Field of Search
UK CL (Edition O) H3P PCCE PCCG PDGS
INT CL[6] H03K 17/16 17/687 17/693

(54) A CMOS transmission gate multiplexer with improved OFF isolation

(57) An improved CMOS transmission gate circuit 50 comprises two cascaded transmission gates 52 and 54 with an earthing NMOS switch 56 connected to the middle node Z. If a positive input transient on line INPUT exceeds the positive power supply potential, charge carriers will be injected into the substrate from the input region (102, figure 7) of the PMOS transistor, but these will be collected by the output region of the transistor (104, figure 7) and shunted to earth through 56. An enclosing transistor structure (figures 8-10) improves charge carrier collection. A p-substrate embodiment is discussed in which the switch 56 is a PMOS device connecting the node Z to Vcc. The multiplexer may be applied to an ADC input selector.

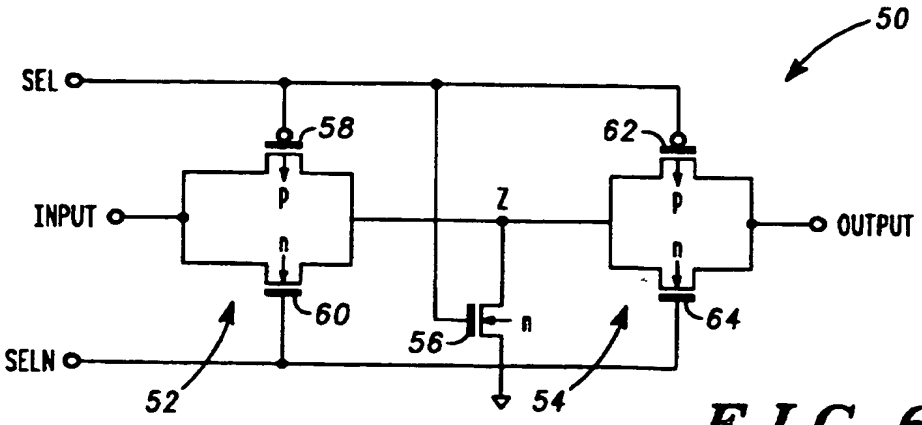

FIG.6

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

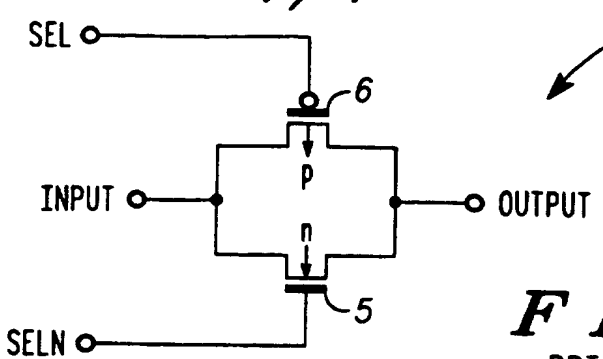

FIG.1
—PRIOR ART—

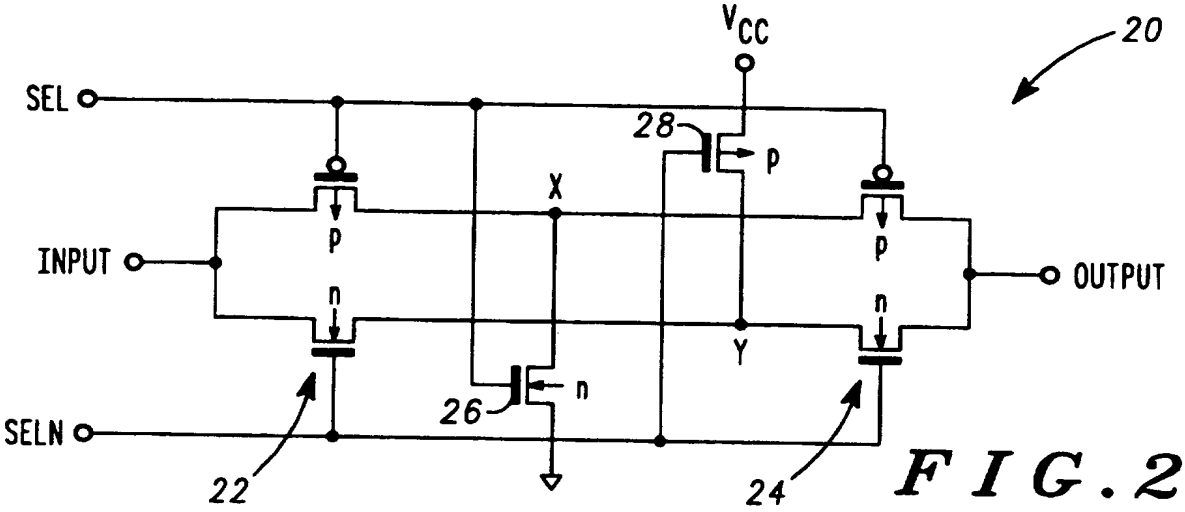

FIG.2
—PRIOR ART—

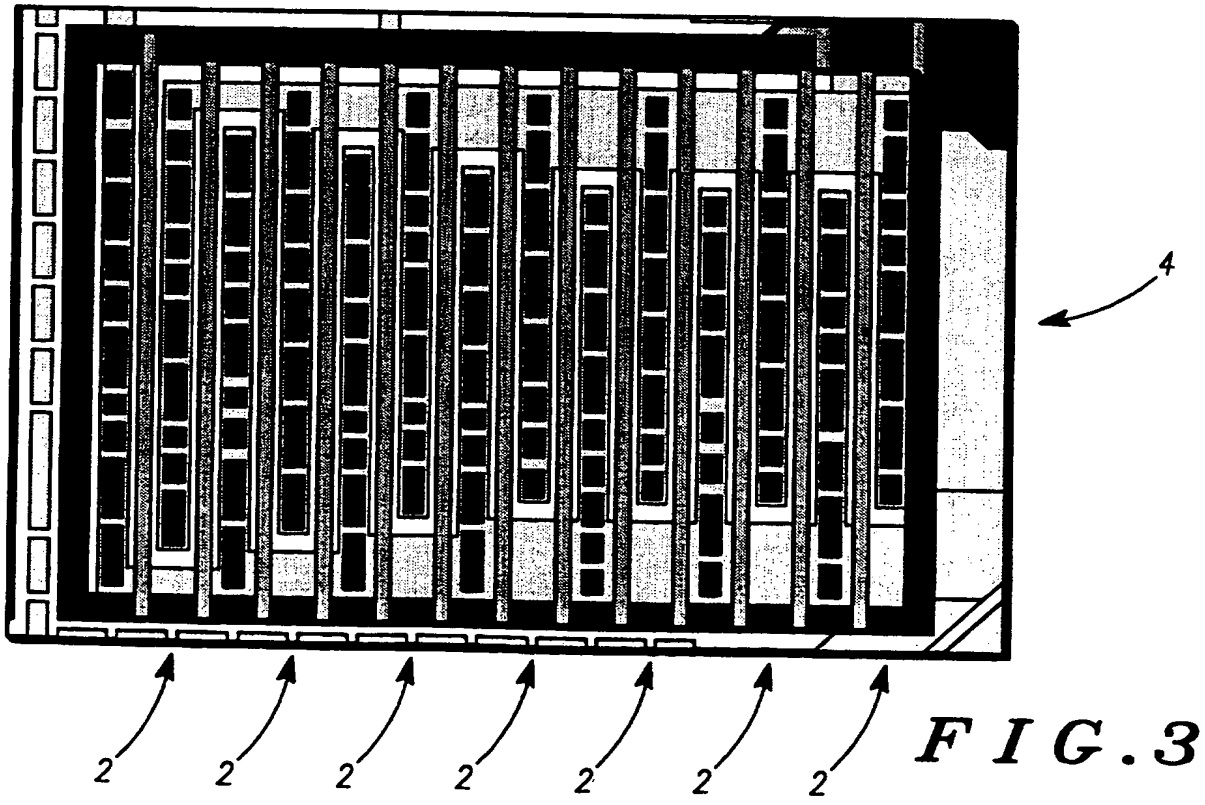

FIG.3

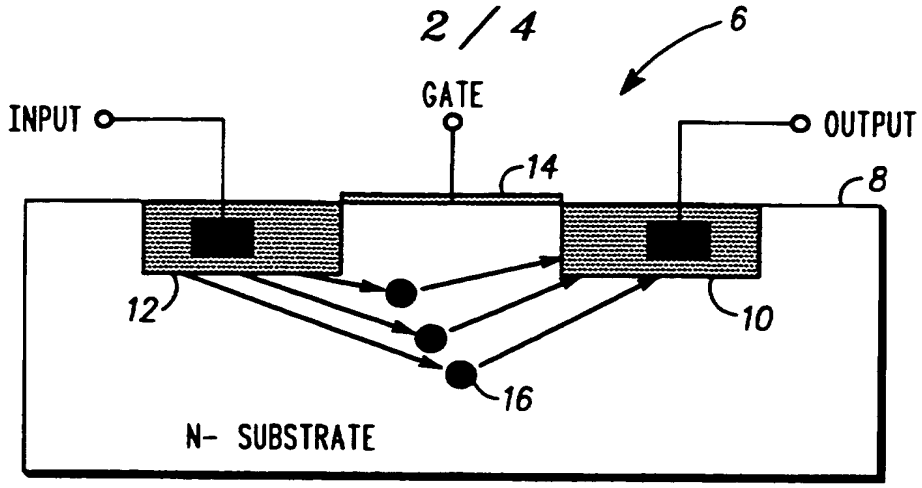

FIG. 4
—PRIOR ART—

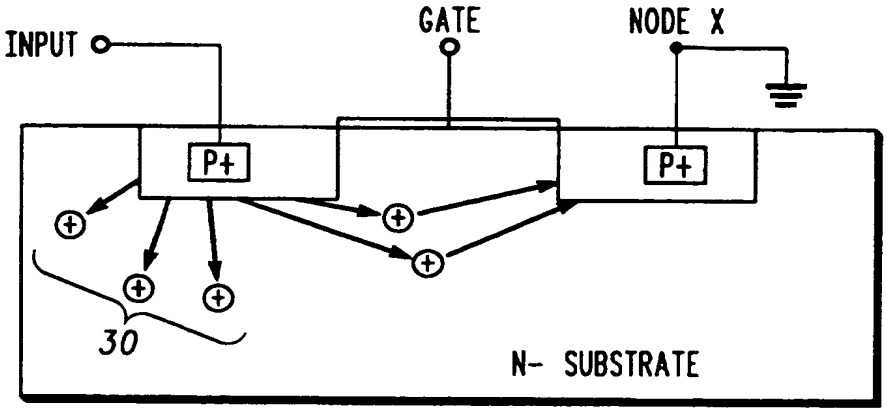

FIG. 5

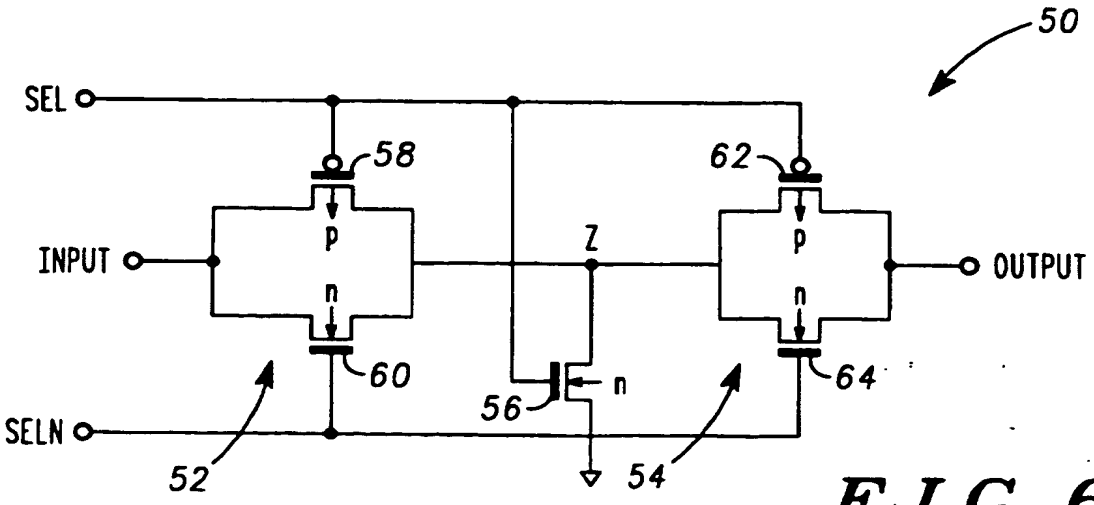

FIG. 6

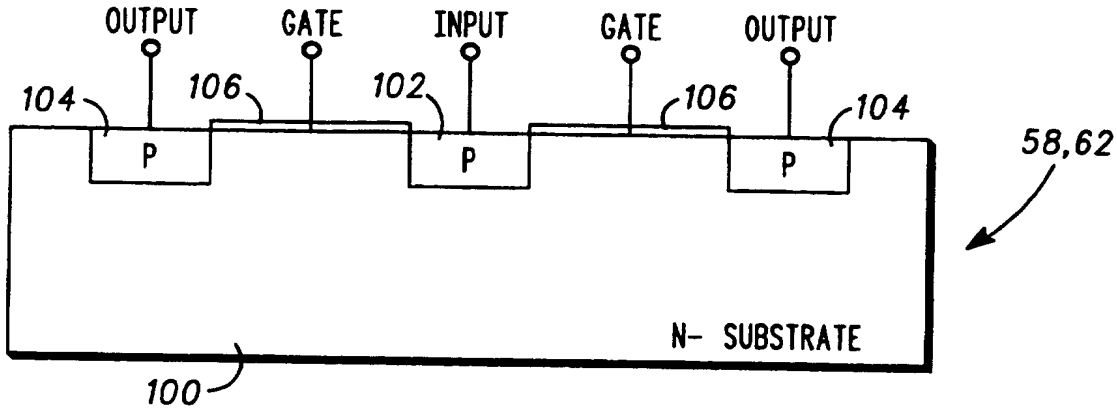

FIG. 7

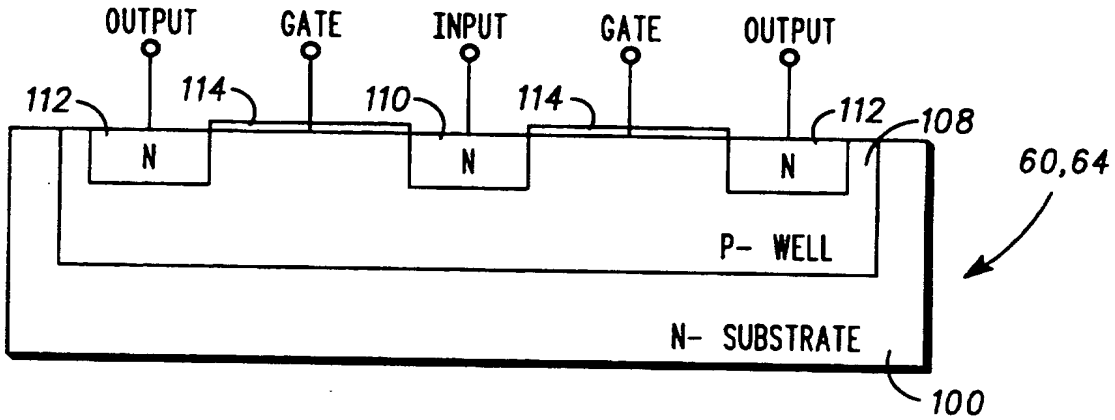

FIG. 8

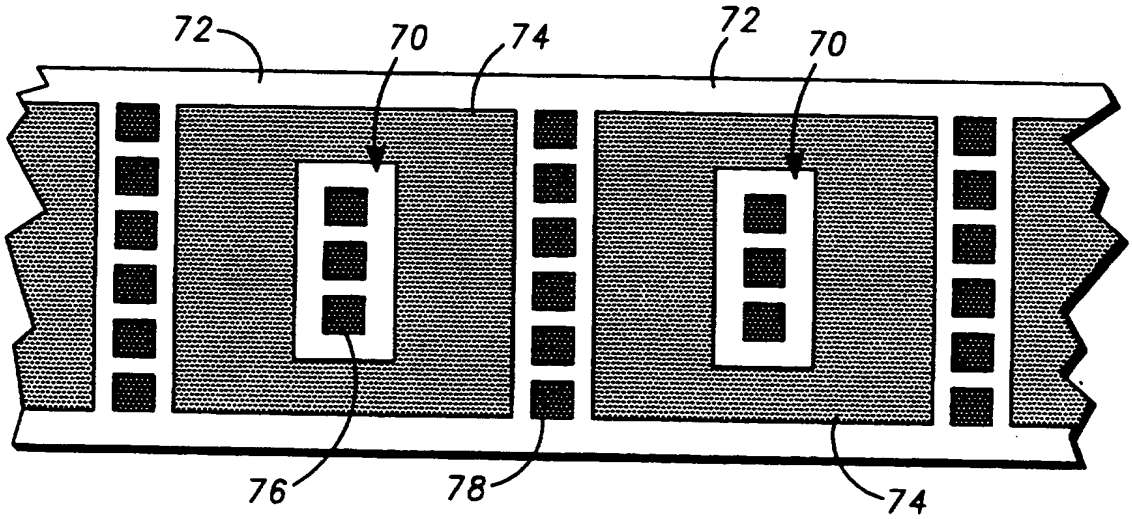

FIG. 9

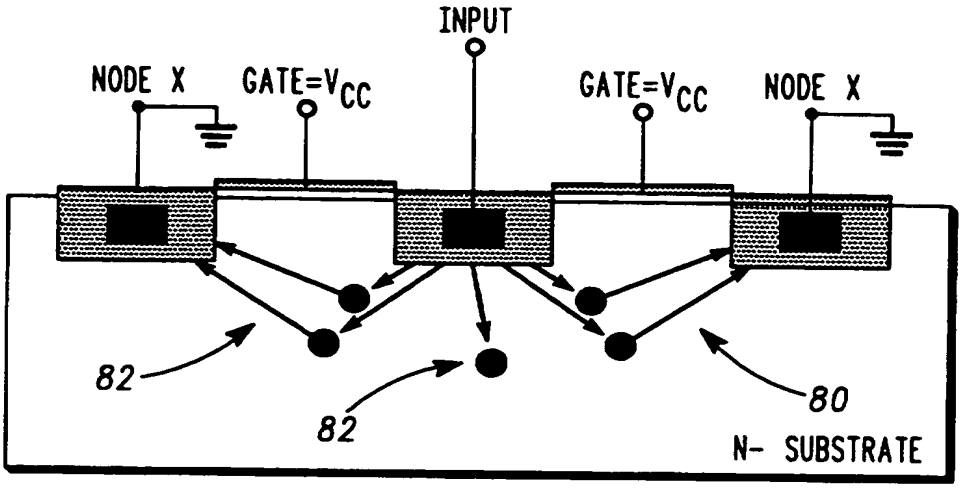

FIG.10

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TRANSMISSION CELL

Field of the Invention

This invention relates to transmission cells for transmittinga signal from an input to an output of the transmission cell in response to a control signal.

Background of the Invention

Transmission cells are used in many different types of integrated circuits (ICs), such as multiplexer and demultiplexer ICs and analog switches.

In certain environments, such as automotive applications, voltage spikes outside the supply voltage range may be coupled to input/output (I/O) pins of the IC. If these voltage spikes arrive at the input of a transmission cell which is closed, they forward bias the PN junctions of the cell's transistors connected to the input. Minority charge carriers are injected into the substrate of the IC producing a parasitic bipolar transistor which impacts internal and external functions and signal levels of the IC. Depending on the function of the IC, this effect can cause logical malfunctions such as RAM cells changing states or analog signals on multiplexer ICs being disturbed.

For example, in a system comprising a plurality of sensors, an analog-to-digital converter (ADC) is required to couple the sensor output signals to a microcontroller. Typically, ADC's have only one input and hence such a system requires a multiplexer. Should a voltage spike occur on one of the transmission cells of the multiplexer such that the input signal is greater than the supply voltage range, all the other transmission cells will be pulled up above the supply voltage range with the result that the microcontroller may malfunction. Thus, when a transmission cell is closed there is required a mechanism to reduce injection currents in the cell and so prevent noise on the other channels of the multiplexer.

In order to suppress these voltage spikes and so reduce the effect of the injection currents, in certain critical applications it is known to use external filter components or networks coupled to the I/O pins of the IC. An external filter may comprise two diodes and two resistors per pin and an additional power supply. The additional power supply is required to ensure that the external diodes are 'on' before the internal diodes which prevents

the internal PN junctions from being forward biased. Such external components are expensive and increase the number of components as well as the printed board space. An integrated immunity solution would therefore be highly preferable compared to external filter networks.

One way to reduce the impact of the injection current effect on transmission cells of a multiplexer/demultiplexer IC, whilst avoiding the need for many additional external components, utilises a transmission cell having two transmission gates (see FIG. 2).

FIG. 1 shows a typical transmission cell having one transmission gate comprising a PMOS and a NMOS transistor coupled in parallel between an input of the transmission cell and an output. A control signal (Sel) and its inverse (SelN) are coupled to respective gate electrodes of the transistors. Since it is impossible to avoid parasitic bipolar coupling across a single-gate transmission cell, the transmission cell shown in FIG. 2, comprises two transmission gates and pull-up and pull-down transistors of the opposite conductivity type which become activated when the transmission cell is closed.

In the two-gate transmission cell, the so-called source of the transmission gates (transmission gates do not have a source in the usual sense) is pulled to the potential which is opposite to the potential of the emitted charge carriers: the charge carriers emitted by the PMOS transistors are positive while the charge carriers emitted by the NMOS transistors are negative. The source therefore becomes a highly attractive collector for the charge carriers emitted by the drain and absorbs them as long as the equipotential lines on which the charge carriers travel end at the source.

Although such a structure reduces the effects of the injection current when the transmission cell is closed, a disadvantage of such a structure is that it requires two transmission gates and two additional transistors and associated connections which increases the die size and cost of such a solution.

An improved transmission cell is therefore required.

Summary of the invention

In accordance with a first aspect of the present invention there is provided a transmission cell for transmitting a signal from an input to an output of the transmission cell in response to a control signal, comprising:

a first transmission gate having an input coupled to the input of the transmission cell and one output coupled to a switch, the switch being switchable between a first state and a second state in response to the control signal; and

a second transmission gate having one input and an output coupled to the output of the transmission cell, the one output of the first transmission gate being coupled to a reference voltage when the switch is in the first state and to the one input of the second transmission gate when the switch is in the second state.

Since only a single switch is used at the output of the first transmission gate, the present invention reduces the number of components compared to the arrangement shown in FIG. 2.

In conventional transmission cell layouts such as the ladder type layout (see FIG. 3), all the ends of the drains (2) as well as typically one broad side (4) are uncovered so that charge carriers emitted into these directions will escape into the substrate or surrounding well. Even a few nano-amperes of cross-coupling current is enough to change, for example, an analog signal of a neighbouring transmission cell by several voltages when the signal line impedance is high. For ADCs, the input impedance is in the range of 10 Mega-ohms. Therefore there is a need to ensure that as many as possible charge carriers of the injection current are collected by the source. With the known types of transmission cell layouts, this is not the case.

The two-gate transmission cell having one of the known layouts therefore has an additional problem in that a significant number of the charge carriers of the injection current are not collected by the source.

Thus, in accordance with a second aspect of the present invention there is provided a transmission cell for transmitting a signal from an input to an output of the transmission cell in response to a control signal, comprising:

a first transmission gate having an input coupled to the input of the transmission cell and an output coupled to a switch, the switch being switchable between a first state and a second state in response to the control signal; and

a second transmission gate having an input and an output coupled to the output of the transmission cell, the output of the first transmission gate being coupled to a reference voltage when the switch is in the first state and to the input of the second transmission gate when the switch is in the second state,

wherein each of the first and second transmission gates comprises:

a first transistor of a first conductivity type;

a second transistor of a second conductivity type;

wherein the first transistor comprises a first semiconductor region of the second conductivity type and first and second regions of the first conductivity type formed in the first semiconductor region and a control region formed between the first and second regions,

wherein the second transistor comprises a second semiconductor region of the first conductivity type and formed in the first semiconductor region and first and second regions of the second conductivity type formed in the second semiconductor region and a control region formed between the first and second regions,

wherein the first regions of the first and second transistors are coupled to the input of the respective transmission gate and the second regions of the first and second transistors are coupled to the output of the respective transmission gate and the control regions of the first and second transistors are coupled to control electrodes of the respective transistors and wherein the second region of each transistor is arranged to surround the control region and the first region of the respective transistor.

In addition to the above advantages described with respect to the first aspect of the invention, this preferred arrangement of having the second region surrounding the first and control regions ensures that substantially most of the charge injected into the substrate due to spikes when the transmission cell is closed are collected by the second region.

Brief Description of the Drawings

Embodiments of the present invention will now be described with reference to the accompanying drawings in which:

FIG. 1 is a schematic circuit diagram of a single-gate transmission cell;

FIG. 2 is a schematic circuit diagram of a two-gate transmission cell;

FIG. 3 is a representation of a transmission cell having a ladder-type layout;

FIG. 4 is a cross-sectional schematic diagram of part of the single-gate transmission cell of FIG. 1 showing the path of injected carriers when the cell is closed;

FIG. 5 is a cross-sectional schematic diagram of part of the two-gate transmission cell of FIG. 2 showing the path of injected carriers when the cell is closed;

FIG. 6 is a schematic circuit diagram of a transmission cell in accordance with the present invention;

FIG. 7 is a cross-sectional schematic diagram of a PMOS transistor which forms part of the transmission cell in accordance with a preferred embodiment of the present invention;

FIG. 8 is a cross-sectional schematic diagram of a NMOS transistor which forms part of the transmission cell in accordance with a preferred embodiment of the present invention;

FIG. 9 is a representation of a transmission cell having a layout in accordance with a preferred embodiment of the present invention; and

FIG. 10 is a cross-sectional schematic diagram of the PMOS transistor of FIG. 7 showing the path of injected carriers when the transmission cell is closed.

Detailed Description of the Drawings

Referring now also to FIG. 4, a PMOS transistor 6 of the single-gate transmission cell 3 of FIG. 1 comprises a substrate of N conductivity type, a first region 12 of P+ conductivity type coupled to the input of the single-gate transmission cell, a second region 10 of P+ conductivity type coupled to the output of the single-gate transmission cell and a gate region 14 between the first 12 and second 10 regions. The transmission cell 3 is open or closed depending on the state of the control signal Sel. When the control signal Sel has a low state, for example when the control signal Sel is at ground reference voltage, the transmission cell 3 is open and the signal at the input is coupled to the signal at the output. When the control signal Sel has a high state, for example when the control signal Sel is at the supply voltage Vcc, the transmission cell 3 is closed.

When transmission cell 3 is closed, if the signal at the input of the transmission cell goes above Vcc (plus a diode drop), minority charge carriers 16 are injected into the substrate of the PMOS transistor 6 as shown in FIG. 4 to produce a parasitic bipolar transistor. Current then flows from the first region 12 to the second region 10. The same is true of the NMOS transistor 5 of transmission cell 3. In a multiplexer, since all the transmission cells are formed in the same substrate 6, all the channels would then be pulled up to Vcc (plus a diode drop).

As mentioned above, FIG. 2 shows a transmission cell 20 having two transmission gates 22, 24, a pull-down transistor 26 and a pull-up transistor 28. Each of the transmission gates 22, 24 comprises a PMOS and a NMOS

transistor whose gate electrodes are coupled to receive a control signal Sel and its inverse respectively.

As with the single-gate transmission cell 3, when the control signal Sel has a low state, the transmission cell 20 is open and the signal at the input is coupled to the signal at the output. When the control signal Sel has a high state, the transmission cell 20 is closed and the pull-up transistor 28 and the pull-down transistor 26 are 'on' or active. Transistor 26 ensures that the source electrode of the PMOS transistor of the first transmission gate 22 is pulled node to ground reference voltage and transistor 28 ensures that the source electrode of the NMOS transistor of the first transmission gate 22 is pulled to the supply voltage Vcc. The result is that voltages at nodes X and Y remain substantially within the supply voltage range.

In the event of a voltage spike, most of the injected charge carriers at the input of the transmission cell 20 are attracted to the respective source electrodes of the PMOS and NMOS transistors of the first transmission gate 22 so that the signal at the output of the second transmission gate 24 and hence at the output of the transmission cell 20 remains valid. FIG. 5 shows the distribution of charge carriers in the PMOS transistor of the first transmission gate 22. However, as mentioned above the transmission cell 20 requires two transmission cells and two pull-up, pull-down transistors and their associated connections. Moreover, some of the charge carriers 30 escape into the substrate which can cause the output of the transmission cell 20 to become invalid.

Referring now to FIG. 6, transmission cell 50 in accordance with a preferred embodiment of the invention for transmitting a signal from an input to an output of the transmission cell in response to a control signal Sel, comprises first 52 and second 54 transmission gates. The first transmission gate 52 has an input coupled to the input of the transmission cell 50 and one output coupled to a switch 56. The second transmission gate 54 has an input and an output, the output being coupled to the output of the transmission cell 50. The switch 56 is switchable between a first state and a second state in response to the control signal Sel such that the one output of the first transmission gate 52 is coupled to a reference voltage when the switch 56 is in the first state and to the input of the second transmission gate 54 when the switch 56 is in the second state.

Each of the first 52 and second 54 transmission gates comprises a first transistor of a first conductivity type and a second transistor of a second conductivity type, both transistors being formed in a semiconductor region or substrate of a second conductivity type. In the preferred embodiment

described herein with reference to FIGs. 6-10, the first transistors 58, 62 are PMOS transistors and the second transistors 60, 64 are NMOS transistors formed in a N type substrate; that is, the first conductivity type is P and the second conductivity type is N. However, it will be appreciated that the present invention also applies when the substrate is P conductivity type; that is when the first conductivity type is N and the second conductivity type is P.

In the embodiment shown in FIG. 6, the first transmission gate 52 comprises a first PMOS transistor 58 and a second NMOS transistor 60. The current electrodes of the first PMOS transistor 58 are coupled in parallel with the current electrodes of the second NMOS transistor 60 between the input of the first transmission gate 52 and its output. The gate electrode of the first PMOS transistor 58 is coupled to receive the control signal Sel and the gate electrode of the second NMOS transistor 60 is coupled to receive the inverse of the control signal SelN. The output of the first transmission gate 52 is coupled to a node Z.

The second transmission gate 54 comprises a first PMOS transistor 62 and a second NMOS transistor 64. The current electrodes of the first PMOS transistor 62 are coupled in parallel with the current electrodes of the second NMOS transistor 64 between the input of the second transmission gate 54 and its output. The gate electrode of the first PMOS transistor 62 is coupled to receive the control signal Sel and the gate electrode of the second NMOS transistor 64 is coupled to receive the inverse of the control signal SelN. The input of the second transmission gate 54 is also coupled to node Z.

The switch 56 comprises a transistor having a first current electrode coupled to node Z and a second current electrode coupled to the reference voltage. A control electrode of switch 56 is coupled to receive the control signal Sel. In the embodiment shown in FIG. 6, the switch 56 is a NMOS transistor and the reference voltage is ground reference voltage.

Referring now also to FIGs. 7 and 8 which show schematic cross-sectional views of the first 58, 62 and second 60, 64 transistors respectively of the first 52 and second 54 transmission gates.

Each of the first transistors 58, 62 of the first 52 and second 54 transmission gates comprises a first semiconductor region 100 of N conductivity type and first 102 and second 104 regions of the P conductivity type formed in the first semiconductor region 100 and a control region 106 formed between the first and second regions. Each of the second transistors 60, 64 of the first 52 and second 54 transmission gates comprises a second semiconductor region 108 of P conductivity type and formed in the first

semiconductor region 100 and first 110 and second 112 regions of N conductivity type formed in the second semiconductor region 108 and a control region 114 formed between the first and second regions. Preferably, the control regions 106, 114 are polysilicon gate regions.

The first regions 102, 110 of the first 58, 62 and second 60, 64 transistors are coupled to the input of the respective transmission gate and the second regions 104, 112 of the first 58, 62 and second60, 64 transistors are coupled to the output of the respective transmission gate. The control regions 106, 114 of the first and second transistors are coupled to the gate electrodes of the respective transistors.

The transmission cell 50 functions as follows.

When the control signal Sel has a low state, which in the preferred embodiment is when the control signal Sel is at the ground reference voltage, all the transistors 58-64 are conducting, switch 56 is 'off' or inactive and the transmission cell 50 is open so that a signal at the input of the transmission cell 50 is transferred to the output of the transmission cell 50.

When the control signal Sel has a high state, which in the preferred embodiment is when the control signal Sel is at a supply voltage Vcc, all the transistors 58-64 are 'off' or non-conducting, switch 56 is conducting or active and the transmission cell 50 is closed. Current injected into the substrate via the first transmission gate 52 and due to spikes on the input of the transmission cell 50 is pulled to the ground reference voltage via switch 56 such that the voltage at node Z is kept substantially within the range of the supply voltage (between -Vbe and Vcc + Vbe) and bipolar coupling effects across the second transmission gate 54 are reduced.

The inventors of the present invention realised that for N conductivity type substrates the need to reduce the injection current is only critical for PMOS transistors, since with NMOS transistors the device is formed in a well of P conductivity type so that only the charge carriers that jump across the channel are a problem and these are less critical since the NMOS diode drop is typically sufficient to drain away the injection current in the NMOS transistor.

The opposite is true for P conductivity type substrates. That is, for P conductivity type substrates the need to reduce the injection current is only critical for NMOS transistors, since with PMOS transistors the device is formed in a well of N conductivity type. A transmission cell in accordance with the present invention formed in a P conductivity type substrate would be substantially the same as the cell 50 described above except that the switch would be a PMOS transistor having a gate electrode coupled to

receive the inverse of the control signal SelN, and a second current electrode coupled to a supply voltage Vcc. The disclosure herein relating to the invention applies equally *mutatis mutandis* to transmission cells formed from a P conductivity type substrate.

Thus, the transmission cell in accordance with the present invention utilises two transmission gates and only one switch to reduce the injection currents in the transmission cell when the transmission cell is closed. By reducing the number of components and connections compared to the transmission cell of FIG. 2, the present invention reduces die size and cost.

Although the transmission cell 50 in accordance with a preferred embodiment of the present invention reduces the effects of the injection of charge carriers with a reduction in components, some of the charge carriers may still escape into the substrate which may cause problems if the impedance of the line connected to the output of the cell 50 is high.

In order to improve the amount of charge carriers trapped by the sources, the transmission cell in accordance with the present invention preferably has a layout as shown in FIG. 9 (see also FIGs. 7 and 8) wherein each drain region 70 (first regions 102, 110) of the transistors which form the first and second transmission gates 52, 54 is completely surrounded by a gate region 74 (control regions 106, 114) and a source region 72 (or second region 104, 112). Regions 76 are drain contact regions and regions 78 are source contact regions.

Such a new layout ensures that the equipotential lines are distributed around the drain region so the chance that charge escapes into the substrate is minimised (see FIG. 10). This means that when the transmission cell 50 is closed (control signal Sel is Vcc), the majority of charges 80 injected into the first transmission gate 52 are coupled to the ground reference voltage and only a very few 82 escape to the substrate. Thus, this preferred layout reduces the consequences of the current injected into the substrate by the voltage spikes outside the supply voltage and ensures that the output of the second transmission gate 54 remains undisturbed.

The transmission cell in accordance with the present invention may be utilised in multiplexer ICs, demultiplexer ICs, in fact any IC requiring a switch or transmission cell.

The signal at the input of the transmission cell in accordance with the present invention will normally be an analog signal. However, the transmission cell in accordance with the present invention may be used as some sort of digital filter in which case the signal at the input would be a digital signal.

Claims

1. A transmission cell for transmitting a signal from an input to an output of the transmission cell in response to a control signal, comprising:

a first transmission gate having an input coupled to the input of the transmission cell and one output coupled to a switch, the switch being switchable between a first state and a second state in response to the control signal; and

a second transmission gate having one input and an output coupled to the output of the transmission cell, the one output of the first transmission gate being coupled to a reference voltage when the switch is in the first state and to the one input of the second transmission gate when the switch is in the second state.

2. A transmission cell according to claim 1 wherein each of the first and second transmission gates comprises:

a first transistor of a first conductivity type;

a second transistor of a second conductivity type;

wherein the first transistor comprises a first semiconductor region of the second conductivity type and first and second regions of the first conductivity type formed in the first semiconductor region and a control region formed between the first and second regions,

wherein the second transistor comprises a second semiconductor region of the first conductivity type and formed in the first semiconductor region and first and second regions of the second conductivity type formed in the second semiconductor region and a control region formed between the first and second regions.

3. A transmission cell according to claim 2 wherein the first region of each transistor is arranged to surround the control region and the second region of the respective transistor.

4. A transmission cell according to claim 2 wherein for each of the first and second transmission gates, the first regions of the first and second transistors are coupled to the input of the respective transmission gate and the second regions of the first and second transistors are coupled to the output of the respective transmission gate and the control regions of the first and second transistors are coupled to control electrodes of the respective transistors.

5. A transmission cell according to claim 4 wherein the second region of each transistor is arranged to surround the control region and the first region of the respective transistor.

6. A transmission cell for transmitting a signal from an input to an output of the transmission cell in response to a control signal, comprising:

a first transmission gate having an input coupled to the input of the transmission cell and an output coupled to a switch, the switch being switchable between a first state and a second state in response to the control signal; and

a second transmission gate having an input and an output coupled to the output of the transmission cell, the output of the first transmission gate being coupled to a reference voltage when the switch is in the first state and to the input of the second transmission gate when the switch is in the second state,

wherein each of the first and second transmission gates comprises:

a first transistor of a first conductivity type;

a second transistor of a second conductivity type;

wherein the first transistor comprises a first semiconductor region of the second conductivity type and first and second regions of the first conductivity type formed in the first semiconductor region and a control region formed between the first and second regions,

wherein the second transistor comprises a second semiconductor region of the first conductivity type and formed in the first semiconductor region and first and second regions of the second conductivity type formed in the second semiconductor region and a control region formed between the first and second regions,

wherein the first regions of the first and second transistors are coupled to the input of the respective transmission gate and the second regions of the first and second transistors are coupled to the output of the respective transmission gate and the control regions of the first and second transistors are coupled to control electrodes of the respective transistors and wherein the second region of each transistor is arranged to surround the control region and the first region of the respective transistor.

7. A transmission cell according to claim 2, 3, 4, 5 or 6 wherein the control region comprises a polysilicon region.

8. A transmission cell according to claim 2, 3, 4, 5, 6 or 7 wherein the first conductivity type is P and the second conductivity type is N and wherein the first semiconductor region comprises a substrate of N conductivity type and the second semiconductor region forms a well in the first semiconductor region.

9. A transmission cell according to any preceding claim wherein the switch comprises a transistor having a control electrode coupled to receive the control signal, a first current electrode coupled to the one output of the first transmission gate and a second current electrode coupled to a reference voltage.

10. A transmission cell according to claim 2 and 9 wherein the switch comprises a transistor of the second conductivity type.

11. A transmission cell according to claim 1 each of the first and second transmission gates comprises a PMOS and a NMOS transistor coupled in parallel between the input and output of the respective transmission gate, the control signal being applied to a gate electrode of the PMOS transistor and an inverse of the control signal being applied to a gate electrode of the PMOS transistor.

12. A transmission cell according to claim 11 wherein the PMOS and NMOS transistors are formed in a substrate of P conductivity type and the switch comprises a NMOS transistor.

13. A transmission cell according to claim 11 wherein the PMOS and NMOS transistors are formed in a substrate of N conductivity type and the switch comprises a PMOS transistor.

14. A multiplexer having a plurality of inputs and an output, the multiplexer comprising a plurality of transmission cells in accordance with any one of the preceding claims, the input of a transmission cell being coupled to a respective one of the plurality of inputs of the multiplexer and the output of a transmission cell being selectively coupled to the output of the multiplexer in response to the control signal.

15. A transmission cell substantially as hereinbefore described with reference to any one of FIGs. 6, 7 or 8 of the accompanying drawings.

The Patent Office

13

Application No: GB 9622633.7
Claims searched: 1-15

Examiner: K. Sylvan
Date of search: 11 December 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H3P (PCCG,PDGS,PCCE)

Int Cl (Ed.6): H03K (17/16,17/693,17/687)

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,Y	US4985703	NEC. See figure 2.	X: 1,2,4,7, 9-11,14,15 Y: 8,12,13
Y	US4985647	NEC. See figure 2.	12
Y	Basic Integrated Circuit Engineering, Hamilton and Howard, McGraw Hill 1975, pages 549-550		8,13

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.